10/774053

Corr

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Steinfeld et al.

Attorney Docket No.:
APL1P300/P3223US1

Patent: 7,129,416 B1

Issued: October 31, 2006

Title: HYBRID GROUND GRID FOR PRINTED CIRCUIT BOARD

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on April 27, 2007 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Aurelia M. Sanchez

REQUEST FOR CERTIFICATE OF CORRECTION OF OFFICE MISTAKE (35 U.S.C. §254, 37 CFR §1.322)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attn: Certificate of Correction

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing. The errors together with the exact page and line number where the errors are shown correctly in the application file are as follows:

SPECIFICATION:

1. Column 4, line 38, change "gird" to --grid--. This appears correctly in the patent application as filed on February 5, 2004 on page 7, paragraph 3, line 2.

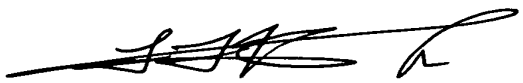
2. Column 8, line 16, change "patch" to --pitch--. This appears correctly in the patent application as filed on February 5, 2004 on page 13, paragraph 37, line 5.

3. Column 8, line 35, change "gird" to --grid--. This appears correctly in the patent application as filed on February 5, 2004 on page 14, paragraph 38, line 1.

Patentee hereby requests expedited issuance of the Certificate of Correction because the error lies with the Office and because the error is clearly disclosed in the records of the Office. As required for expedited issuance, enclosed is documentation that unequivocally supports the patentee's assertion without needing reference to the patent file wrapper.

It is noted that the above-identified errors were printing errors that apparently occurred during the printing process. Accordingly, it is believed that no fees are due in connection with the filing of this Request for Certificate of Correction. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. APL1P300).

Respectfully submitted,
BEYER WEAVER LLP



Frank T. Kalinski, II.
Registration No. 44,177

P.O. Box 70250
Oakland, CA 94612-0250
408-255-8001

[0013] Other aspects and advantages of the invention will become apparent from the following detailed description and accompanying drawings which illustrate, by way of example, the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The following detailed description will be more readily understood in conjunction with the accompanying drawings, in which:

[0015] Figs. 1(a)-1(d) are simplified schematic depictions of a conventional printed circuit board (PCB) having a convention ground grid as is used to mount electronic components.

[0016] Figs. 2(a)-2(b) are simplified schematic depictions of conventional PCB's that illustrate some of the problems encountered when a convention ground grid as is used to mount electronic components.

[0017] Figs. 3(a)-3(f) are simplified schematic depictions of a hybrid ground grid embodiment constructed in accordance with the principles of the invention.

[0018] Figs. 4(a)-4(c) are simplified schematic depictions of another hybrid ground grid embodiment constructed in accordance with the principles of the invention.

[0019] Figs. 5(a)-5(c) are simplified schematic depictions of another approach for establishing a hybrid ground grid embodiment constructed in accordance with the principles of the invention.

[0020] Fig. 6 provides some simplified illustrations of a ground grid structure constructed in accordance with the principles of the invention.

[0021] Fig. 7 is a simplified schematic depiction of a track pad implementation incorporating a ground grid constructed in accordance with the principles of the invention.

help to reduce EMC problems. Additionally, as is readily appreciated by those having ordinary skill in the art, in a conventional circuit board having ground plane, when current passes through signal line connected with a component or device a return current path is formed in the ground plane which passes directly underneath (or overhead) the signal line. Thus, in a conventional configuration, the signal and return current propagation paths are substantially mirror images of each other. This condition of mirror image signal and return paths may not always be possible when a ground grid of the present invention is employed. However, by constructing a ground grid having a densely packed pattern of very small ringlets it is possible to construct a return path that very nearly matches that of the signal path. Thus, by forming a tightly packed arrangement of very small ringlets, small loop area return electrical paths can be formed. The inventors contemplate that larger ringlets can be used, but this is achieved at the cost of reduced EMC performance for the larger loop areas of the board.

[0036] The inventors specifically point out that the embodiment of Fig. 3(f) is depicted on the top surface of a circuit board. Other embodiments of the invention can use three-dimensional implementations to generate source lines and their associated return lines in a three-dimensional configuration.

[0037] In one implementation a ringlet 331 comprises a portion of a ground grid such as described elsewhere herein. Each ringlet 331 defines an area **A**. In some embodiments, this area **A** is reduced to a minimum possible area to optimize electromagnetic compatibility (EMC) performance of the ground grid. By minimizing the grid "pitch" (i.e., minimizing the grid ringlet areas **A**) EMC performance can be optimized. Additionally, in some embodiments, a ratio of about 10 (or fewer) signal lines to each associated ringlet 331 is preferred. Thus, the use of a hybrid ground grid allows a user to implement a denser ground grid and hence better EMC (Electromagnetic Compatibility) performance. Implementations of hybrid ground grids constructed in accordance with the principles of the invention can also vary in the size of the ringlets in different areas of a circuit board layout. For example, in areas having a high component

and/or signal line density, larger ringlets could be used to accommodate component and signal line placement. Whereas in other portions of the board, denser patterns of smaller ringlet size can be used to accommodate a minimum ringlet dimension. Such configurations can "have the best of both worlds" as it were having both improved areas for components and signal lines as well as availability of improved return paths due to the presence of densely packed small ringlets.

[0038] Fig. 4(a) depicts another bi-directional ground grid approach. Fig. 4(a) shows a top plan view of a top surface 400 which can be implemented with a board. For example, it could be used in place of 301T of board 300 in Fig. 3(a). Fig. 4(a) depicts another pattern of hybrid ground traces 401 that can be formed on the surface 301T. Again, the hybrid ground traces are configured such that at least some of the ground traces (formed on a level of the board) are oriented in a different direction from other ground traces formed on the same level of the board. The hybrid ground traces 401 of Fig. 4(a) are configured having at least two groups 411, 412 of ground traces, each being oriented in different directions.

[0039] Still referring to Fig. 4(a), the hybrid ground traces 401 are arranged in a hybrid configuration so that a first group 411 of electrical ground traces is arranged in a transverse relationship with a second group 412 of electrical ground traces. In the depicted configuration, the first group 411 of electrical ground traces is arranged so that all the ground traces in the group 411 are substantially parallel to each other. The depicted group 411 is in the so-called "Y"-axis configuration. The second group 412 of electrical ground traces is arranged so that all the ground traces in the group 412 are substantially parallel to each other. The depicted group 412 is in a diagonal configuration. Again, the first group 411 can optionally be electrically connected with the second group 412 is some places. The depicted ground traces are typically formed of a conductive material (e.g., copper). Again, transverse is intended to mean that the orientation of the traces of at least one group (e.g., the first group 411) is not parallel to the orientation of at least one other group of traces (e.g., the second group 412) as shown, for example

PTO/SB/44 (10-96)
Approved for use through 6/30/99. OMB 0651-0033
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PT-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,129,416 B1 Page 1 of 1

DATED : October 31, 2006

INVENTOR(S) : Steinfeld et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Specification:

Column 4, line 38, change "gird" to --grid--.

Column 8, line 16, change "patch" to --pitch--.

Column 8, line 35, change "gird" to --grid--.

MAILING ADDRESS OF SENDER:

PATENT NO. 7,129,416 B1

Frank T. Kalinski, II.
BEYER WEAVER LLP
P.O. Box 70250
Oakland, CA 94612-0250

No. of Additional Copies

1